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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,875	12/05/2000	Satoshi Ishida	2933SE-64-CON	9363

22442 7590 02/27/2003

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EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	12

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

P-S

Office Action Summary	Application No.	Applicant(s)	
	09/730,875	ISHIDA ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. in view of Ono et al. (PTO-1449 filed on 12/5/00).

Tsai et al. disclose a thin film transistor in fig. 11. It comprises: an insulator substrate [71]; a gate electrode [72] located on the insulator substrate; a gate insulator film [73] provided above the insulator substrate and the gate electrode; and a polycrystalline silicon film [74, 176] located on the gate insulator film, the polycrystalline silicon film being formed by laser annealing step on a surface of an amorphous layer; the gate electrode having a center portion with a flat surface.

Tsai et al. differ from the claimed invention by not showing a pair of tapered end portions with inclined surfaces and an angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 10° to 40°.

Ono et al. (fig. 25) show a tapered end portion of a gate electrode [2] with inclined surface and an angle θ_g between the inclined surface of the tapered end portion of the gate electrode [2] and a surface of the insulator substrate [1] being set to 10° (col. 18, lines 1-11).

Since both Tsai et al. and Ono et al. teach a thin film transistor with a bottom gate electrode, it would have been obvious to have the tapered end portion of the gate

electrode of Ono et al. in each side of the gate electrode of Tsai et al. because it prevents the generation of crack at the portion of the gate insulating film that overlaying the gate electrode.

It is inherent that the combined device shows a uniform grain size of the polycrystalline silicon film formed above the center portion and the pair of tapered end portions of the gate electrode because the gate electrode of the combined device having a center portion with a flat surface and a pair of tapered end portions with inclined surfaces, an angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set to 10°.

Since the combined device shows the angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set to 10°, it is inherent that a gate withstand voltage of the thin film transistor is secured and the inclined surfaces of the pair of tapered end portions are prevented from increasing.

3. Applicant's arguments filed 1/28/03 have been fully considered but they are not persuasive.

It is urged, in page 4 of the remarks, that an angle smaller than 10° causes the disadvantages recited at page 22, line 30 to page 23, line 3 of the present specification and makes it difficult to control a gate width of TFT. However, page 22, line 29 to page 23, line 3 of the present specification discloses an angle smaller than 5 ° means an increased surface of the tapered portion 76b, which causes a variation in the membranous of the polycrystalline silicon film 81. The specification never discloses an

angle between 5 to 10° causes disadvantages to the device and makes it difficult to control a gate line width of TFT.

It is urged, in page 4 of the remarks, that Ono et al. never disclose setting the taper angle of the end portion within 10° to 40° in order to acquire a uniform grain size of the polycrystalline silicon film above the center portion and the pair of tapered end portions. However, Ono et al. teach a taper angle of the end portion of a gate electrode can be 10°. Therefore, the taper angle of each of the end portions of the gate electrode of the combined device of Tsai et al. and Ono et al. can also be 10°. Since the gate electrode structure of the combined device is similar to that of the claimed invention, it is inherent that a uniform grain size of the polycrystalline silicon would be form above the center portion and the pair of tapered end portions of the gate electrode of the combined device. It is believed that the combined device of Tsai et al. and Ono et al. meets the limitation of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
February 21, 2003

Steven Loke